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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,443	03/30/2004	Vishal Sarin	2102397-992980	5465
26379	7590	08/25/2005	EXAMINER	
DLA PIPER RUDNICK GRAY CARY US, LLP			LUU, PHO M	
2000 UNIVERSITY AVENUE			ART UNIT	
E. PALO ALTO, CA 94303-2248			PAPER NUMBER	

2824

DATE MAILED: 08/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/814,443

Applicant(s)

SARIN ET AL.

Examiner

Pho M. Luu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2-9 is/are allowed.
- 6) ☒ Claim(s) 1 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input checked="" type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____ | 6) <input checked="" type="checkbox"/> Other: <u>Search History</u> . |

DETAILED ACTION

1. This office action acknowledges receipt of the following items from the Applicant:
The Specification, Claims, Abstract, Drawing and Oath or Declaration filed on 30 March 2003.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because it uses the phrase "**system includes**" in lines 3-4, which is implied. Correction is required. See MPEP § 608.01(b).

4. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Haddad et al. (US. 6,275,415).

Regarding independent claim 1, Haddad et al. in Figure 6 discloses a method for programming (see column 1, lines 8-9) a memory cell comprising:

applying an increment current (current I_1 , I_2 , I_3 , I_4) to bit-lines (bit line BL which having contain total of bit line current $I_{BL} = I_1 + I_2 + I_3 + I_4$) of selected memory cells (cells 602, 604, 606, 608) during programming of the selected memory cells (for example, a programming current I_2 flows through the cell 604 from ground to source and drain and through bit-line BL which have the bit line current $I_{BL} = I_2$ only, see column 4, lines 30-35), the incremental current being substantially equal to leakage current of the bit line (see column 4, lines 30-43). To be more specifically, for example, a programming voltage is apply to the control gate of transistor cell 604 which is turn on and the current I_2 flow through cell 604 (selected cell) equal to bit line current ($I_{BL} = I_2$) and other unselected cell (602, 606, 608) are overerased with voltage will be very low

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and leakage current I_1 , I_3 and I_4 could flow through cells 602, 606 and 608 which means the bit line current I_{BL} then equal to I_2 and leakage current I_1 , I_3 and I_4 . (see column 4, lines 30-55).

Allowable Subject Matter

7. Claims 2-10 is allowed.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to: "detecting a leakage current on the bit line of the second memory array and applying an incremental current to the bit lines of the first memory array substantially equal to the detected current during programming of the first memory array" as claimed in the independent claim 2; or

"a first circuit having an input coupled to a bit line of a first one of the memory array and having an output coupled to a bit line of a second one of the memory array to apply a voltage on the bit line of the memory array equal to a voltage on the bit line of the first memory array during programming of the first memory array" as claimed in the independent claim 3; or

"the detector having a first input coupled to bit line of a second memory array having a second input coupled to the first output of the current source to receive the first current and having an output coupled to the bit line of the first memory array to apply a voltage on the bit line of the first memory array equal to the voltage on the bit line of the

second memory array in the first mode and the first and second current being substantially equal” as claimed in the independent claim 10.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. The examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for the organization where this application or proceeding is assigned is 703.872.9306 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PL
PML
16 August 2005


